CLAIMS

What is claimed is:

1. A memory device comprising:

a storage array comprised of a plurality of memory cells organized into an array of rows;

an interface buffer coupled to the storage array, and having a first interface to couple the memory device to a first memory bus to couple the memory device to an external memory controller; and

refresh logic associated with the interface buffer to carry out a refresh operation on a row within the storage array during a period of time in which there are no transactions carried out by the external memory controller on the first memory bus that involve the storage array.

2. The memory device of claim 1, wherein the refresh logic is a component of the interface buffer, and wherein the memory device is comprised of a circuitboard to which is attached at least one integrated circuit that comprises the storage array and at least one integrated circuit that comprises the interface buffer.

3. The memory device of claim 1, wherein the first memory bus provides a point-to-point connection between the memory device and the external memory controller, the interface buffer has a second interface to couple the memory device to a second memory bus to provide a point-to-point connection between the memory device and another memory device, and the interface buffer passes through bus activity between the first and second memory busses that does not involve the storage array.

4. The memory device of claim 3, wherein both a transfer of data between the external memory controller and the first interface of the interface buffer and a transfer of data between the second interface of the interface buffer and the other memory device occur with data transmitted in a packets.

5. The memory device of claim 3, wherein the refresh logic monitors activity on the first memory bus to identify a dead time in which no commands are received from the first memory bus involving the storage array, providing an opportunity for the refresh logic to opportunistically carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array.

6. The memory device of claim 5, wherein the refresh logic carries out a refresh operation on a row within the storage array during a period of time in which a transaction between the external memory controller and the other memory device occurs.

7. The memory device of claim 3, wherein the refresh logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the storage array will be transmitted by the external memory controller, providing an opportunity for the refresh logic to carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array.

8. The memory device of claim 3, wherein the refresh logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing an opportunity for the refresh logic to opportunistically carry out a refresh operation on

a row within the storage array without delaying the carrying out of an access command involving the storage array.

9. An interface buffer comprising:

a local interface to a storage array comprised of a plurality of memory cells organized into an array of rows;

a first interface to couple the storage array to a first memory bus to couple the storage array to an external memory controller wherein the first memory bus provides a point-to-point connection between the first interface and the external memory controller;

a second interface to couple the storage array to a second memory bus to couple the second interface to another interface buffer to couple another storage array to the external memory controller through the interface buffer wherein the second memory bus provides a point-to-point connection between the second interface and the other interface buffer; and

refresh logic to carry out a refresh operation on a row within the storage array during a period of time in which there are no transactions carried out by the external memory controller on the first memory bus that involve the storage array.

10. The interface buffer of claim 9, wherein the interface buffer is comprised of at least one integrated circuit, the storage array is comprised of at least one integrated circuit, and both the at least one integrated circuit comprising the interface buffer and the at least one integrated circuit comprising the storage array are attached to a circuitboard to comprise a memory device.

11. The interface buffer of claim 10, wherein the first interface is coupled to the first memory bus and the second interface is coupled to the second memory bus when the

memory device is coupled to another circuitboard to which the external memory controller is attached.

12. The interface buffer of claim 9, wherein both a transfer of data between the external memory controller and the first interface and a transfer of data between the second interface and the other interface buffer occur with data transmitted in a packets.

13. The memory device of claim 9, wherein the refresh logic monitors activity on the first memory bus to identify a dead time in which no commands are received from the first memory bus involving the storage array, providing an opportunity for the refresh logic to opportunistically carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array.

14. The memory device of claim 13, wherein the refresh logic carries out a refresh operation on a row within the storage array during a period of time in which a transaction between the external memory controller and the other storage array occurs.

15. The memory device of claim 9, wherein the refresh logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the storage array will be transmitted by the external memory controller, providing an opportunity for the refresh logic to carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array.

16. The memory device of claim 9, wherein the refresh logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing

an opportunity for the refresh logic to opportunistically carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array.

17. A memory system comprising:

a memory controller;

a first memory bus coupled to the memory controller;

a first memory device having a first storage array comprised of a plurality of memory cells organized into rows and a first interface buffer coupled within the first memory device to the first storage array, wherein the first interface buffer provides a first interface by which the first memory device is coupled to the first memory bus forming a point-to-point connection between the memory controller and the first interface, a second interface, and a first refresh logic to carry out a refresh operation on a row within the first storage array during a period of time in which there are no transactions carried out by the memory controller on the first memory bus that involve the first storage array;

a second memory bus coupled to the second interface; and

a second memory device having a second storage array comprised of a plurality of memory cells organized into rows and a second interface buffer coupled within the second memory device to the second storage array, wherein the second interface buffer provides a third interface by which the second memory device is coupled to the second memory bus forming a point-to-point connection between the third interface and the second interface, and a second refresh logic to carry out a refresh operation on a row within the second storage array during a period of time in which there are no transactions carried out by the memory controller on the second memory bus that involve the second storage array.

18. The memory system of claim 17, wherein the first interface buffer passes through bus activity between the first and second memory busses that does not involve the first storage array.

19. The memory system of claim 18, wherein both a transfer of data between the memory controller and the first interface and a transfer of data between the second interface and the third interface occur with data transmitted in a packets.

20. The memory system of claim 17, wherein the first refresh logic monitors activity on the first memory bus to identify a dead time in which no commands are received from the first memory bus involving the first storage array, providing an opportunity for the first refresh logic to opportunistically carry out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the first storage array.

21. The memory system of claim 20, wherein the first refresh logic carries out a refresh operation on a row within the first storage array during a period of time in which a transaction between the memory controller and the second storage array occurs.

22. The memory system of claim 20, wherein the second refresh logic monitors activity on the second memory bus to identify a dead time in which no commands are received from the second memory bus involving the second storage array, providing an opportunity for the second refresh logic to opportunistically carry out a refresh operation on a row within the second storage array in parallel with the first refresh logic carrying out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the second storage array.

23. The memory system of claim 17, wherein the first refresh logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the first storage array will be transmitted by the memory controller, providing an opportunity for the first refresh logic to carry out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the first storage array.

24. The memory system of claim 23, wherein the second refresh logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the second storage array will be transmitted by the memory controller, providing an opportunity for the second refresh logic to carry out a refresh operation on a row within the second storage array in parallel with the second refresh logic carrying out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the second storage array.

25. The memory system of claim 17, wherein the first refresh logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing an opportunity for the first refresh logic to opportunistically carry out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the first storage array.

26. The memory system of claim 25, wherein the first refresh logic monitors the second memory bus for the occurrence of a powering down of the second memory bus, providing an opportunity for the second refresh logic to opportunistically carry out a refresh operation on a row within the second storage array in parallel with the second refresh logic carrying out a refresh operation on a row within the second storage array without delaying the carrying out of an access command involving the second storage array.

27. A computer system comprising:

a processor;

a disk storage device coupled to the processor

a memory controller coupled to the processor;

a first memory bus coupled to the memory controller;

a first memory device having a first storage array comprised of a plurality of memory cells organized into rows and a first interface buffer coupled within the first memory device to the first storage array, wherein the first interface buffer provides a first interface by which the first memory device is coupled to the first memory bus forming a point-to-point connection between the memory controller and the first interface, a second interface, and a first refresh logic to carry out a refresh operation on a row within the first storage array during a period of time in which there are no transactions carried out by the memory controller on the first memory bus that involve the first storage array;

a second memory bus coupled to the second interface; and

a second memory device having a second storage array comprised of a plurality of memory cells organized into rows and a second interface buffer coupled within the second memory device to the second storage array, wherein the second interface buffer provides a third interface by which the second memory device is coupled to the second memory bus forming a point-to-point connection between the third interface and the second interface, and a second refresh logic to carry out a refresh operation on a row within the second storage array during a period of time in which there are no transactions carried out by the memory controller on the second memory bus that involve the second storage array.

28. The computer system of claim 27, wherein the first refresh logic carries out a refresh operation on a row within the first storage array during a period of time in which a transaction between the memory controller and the second storage array occurs.

29. The computer system of claim 27, wherein the first refresh logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the first storage array will be transmitted by the memory controller, providing an opportunity for the first refresh logic to carry out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the first storage array.

30. The computer system of claim 29, wherein the memory controller is further comprised of a control register programmable by the processor to enable the transmitting of a signal by the memory controller to the first refresh logic to identify a dead time.

31. The computer system of claim 27, wherein the first refresh logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing an opportunity for the first refresh logic to opportunistically carry out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the first storage array.

32. A method comprising:

determining whether or not a memory device coupled to a memory controller via a memory bus possesses a first refresh logic independent of a second refresh logic comprising the memory controller;

programming the memory controller to examine queued memory access commands and signal the first refresh logic to identify a dead time in which the memory controller will not transmit a command involving a storage array within the memory device, providing an opportunity for the first refresh logic to carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array, if the memory controller supports examining queued memory access commands and the memory device possesses the first refresh logic; and

programming the memory controller to power down the memory bus, providing an opportunity for the first refresh logic to carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array, if the memory controller supports examining queued memory access commands and the memory device possesses the first refresh logic.

33. The method of claim 32, further comprising:

signaling the first refresh logic that the first refresh logic controls the timing of refresh operations and powering down the memory bus, if the memory controller supports examining queued memory access commands and the memory device possesses the first refresh logic; and

powering up the memory bus and signaling the first refresh logic that the second refresh logic controls the timing of refresh operations, if the memory controller supports examining queued memory access commands and the memory device possesses the first refresh logic.

34. A method comprising:

checking whether or not there is an access operation to carry out;

carrying out an access operation if the check for an access operation to carry out reveals that there is an access operation to carry out;

carrying out a refresh operation under the control of refresh logic within an interface buffer of a memory device if the check for an access operation to carry out reveals that there is not an access operation to carry out and a refresh operation is needed; and

signaling a memory controller coupled to the memory device via a memory bus that the memory device is unable to carry out an access operation if the memory controller transmits an access command to the memory device during the occurrence of a refresh operation under the control of the refresh logic within the interface buffer within the memory device.

35. The method of claim 34, further comprising:

checking whether or not the memory bus is powered down; and

carrying out a refresh operation under the control of refresh logic within an interface buffer of the memory device if the check for the powering down of the memory bus reveals that the memory bus is powered down and a refresh operation is needed.

36. A machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to:

program a memory controller to which the processor is coupled to determine whether or not a memory device coupled to the memory controller via a memory bus possesses a first refresh logic independent of a second refresh logic comprising the memory controller;

program the memory controller to examine queued memory access commands and signal the first refresh logic to identify a dead time in which the memory controller will not transmit a command involving a storage array within the memory device, providing an opportunity for the first refresh logic to carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array, if the memory controller supports examining queued memory access commands and the memory device possesses the first refresh logic; and

program the memory controller to power down the memory bus, providing an opportunity for the first refresh logic to carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array, if the memory controller supports examining queued memory access commands and the memory device possesses the first refresh logic.

37. The machine-accessible medium of claim 36, further causing the processor to:

signal the first refresh logic that the first refresh logic controls the timing of refresh operations and power down the memory bus, if the memory controller supports examining queued memory access commands and the memory device possesses the first refresh logic; and

power up the memory bus and signal the first refresh logic that the second refresh logic controls the timing of refresh operations, if the memory controller supports examining queued memory access commands and the memory device possesses the first refresh logic.